of which are incorporated herein by reference, promises both high resolution and reduced conversion time.

It is on the background hitherto described, that the present invention was conceived. The invention described below provides a basis for increasing the rate of sampling digitally at the FPP level, without compromising the resolution of each pixel.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is schematic description of the main structural features of an IR sensor system in which the invention is implemented;

Fig. 2 is a flow chart describing schematically the process of the invention;

Fig. 3A is a schematic description of the pixel charge converting circuit of the invention;

Fig. 3B is a charge DAC implementation in accordance with an embodiment of the invention;

Fig. 3C is another charge DAC implementation in accordance with an embodiment of the invention;

Fig. 4 is an implementation of a pixel charge converting circuit of the invention adapted for an array of pixels;

Fig. 5A is a detailed implementation of the circuit described in Fig. 4;

Fig. 5B is a description of the main wave - shape forms in the circuit of Fig. 5A, implemented in the course of one conversion cycle;

Fig. 6. is a schematic description of the interconnections existing between the main components of the imaging system, in accordance with the present invention.

FPP pixel charge digital conversion

The charge accumulated in the pixel in the FPP of the invention is according to the present invention converted to a digital form by a circuit modified from Van De Plassche, cited above. The original circuit, known as a dual ramp single slope converter, converts input voltage into a digital number. The modification of the circuit to a charge converter circuit, and the function thereof are described in reference to **Fig. 3A**. The charge ADC **52** is composed of comparator **66**, charge output digital – to - analog converter (DAC) **62** and of controller **64**. The input port of ADC **52** is line **67**, which connects between the output port of the DAC **62** and comparator **66**. Qpx, the charge to be converted, is stored in pixel capacitor **60**. DAC **62** produces a charge of opposite polarity, the value of which is controlled digitally by the controller **64**. The digital control value (in bits) which eliminates Qpx (as indicated by the comparator **66** output) is the conversion output. Two exemplary implementations of a charge DAC of the invention are described in **Figs. 3B** and **3C** to which reference is now made. In **Fig. 3B** a DAC implementation is described in which the charge for elimination of the Qpx is provided by a set of several capacitors such as capacitor **68**, used in a successive approximation mode. It is also possible to use only the smallest capacitor, switching it many times and counting the number of switching necessary to eliminate the converted charge. In Fig. **3C**, the required charges are achieved by switching-on the relevant current sources, e.g. source **69**, for a given time, producing charge packets accordingly.

However, in practice, the pixels are arranged in the framework of a matrix of rows and columns which may be long such that certain implications are inevitable trying to adapt a solitary pixel ADC application to a pixel array application, such as a column of the array. Accordingly, the following two concerns must be dealt with. First, the long column line adds a parasitic capacitance, Ccl, the value of which is about one order of magnitude larger then the pixel capacitor Cpx. Second, during the conversion, a cross-talk exists between adjacent column lines, impairing the function of the matrix.

In accordance with the present invention, an integrator, the intput of which is a virtual ground, is added as a first stage of the comparator of the charge ADC circuit. This architectural feature helps to overcome the above mentioned problems as the column line in this configuration becomes connected to a virtual ground. Such a configuration is described in **Fig. 4** to which reference is now made. Integrator **70**, is disposed between the comparator **72** and the column line **74**, The charge to be converted is stored in the integrator's capacitor **76**, whereas the charge injected from DAC **78** into the virtual ground, eliminates this charge as described above.

The use of an FPA of the invention is typically in IR imaging applications, in which accurate reference to the absolute temperature of a pixel is not required. Rather, in an IR imaging application, the accuracy of the differences among the different pixels is the matter of relevance. Accurate variability measurement and conversion can be supported by the "dual ramp single slope ADC" used in some embodiments of the present invention.

The "dual ramp single slope ADC" employs a quantification cycle which implements two steps. In the first step MS (most significant) part of the

numeric value is determined, and in a second step, LS (least significant) part of the numeric value of the charge is determined. The two parts of the digital values of the measured quantity must be combined to form a complete digital word, as will be explained later on. In the framework of a pixel array, the readout and quantification are performed in the context of columns and rows as has been discussed above, and will be further explained with reference to **Figs. 5A** and **5B**. In **Fig. 5A** is shown an ADC circuit in accordance with a preferred embodiment of the invention, the function of which is explained with reference to the conversion cycle and switching sequences described in **Fig. 5B**.

At time t_0, the quiescent output voltage of integrator **90**, is forced by closing momentarily switch S1 **91** to Vpch, (pre - charge voltage), which is also the reference voltage for comparator **92**. Closing momentarily switch S3 **94** at time t_1, the charge of a pixel, accumulated in capacitor Cpxl **96**, is transferred to integrator **90**, lowering the output voltage accordingly. Closing switch S4 **98** at time t_2, a constant current source is established by the combination of a linear ramp voltage (ramp **148** of **Fig. 5B**), the capacitor C1 **100** and the virtual ground of the integrator. Switch S5 **102** closes simultaneously with switch S4 **98**. Counter **104**, which has been reset earlier, starts counting the clock pulses while the integrator output goes up linearly. Reaching Vpch at time t_3 the integrator activates the comparator. The period $t_3 - t_2$ is a true indication of the signal to be measured. Yet, the output of the comparator is synchronized to the next clock, and only then it opens switch **98** and samples the counter reading (switch S5 **102** remains closed until t_4 in

order to serve other ADCs). As a result, the output of the integrator continues to rise for a period Δt (in **Fig. 5B**), so that the counter reading provides only the MS count, and a value, proportional to Δt should be subtracted with higher resolution. This is done by resetting counter **104** and closing again switch S5 **102** and switch S4 **98** at time t_5, which connects a second ramp (ramp **150** in **Fig. 5B**), the slope of which is positive and slower.

The output of the integrator goes down and reaches Vpch at time t_6, disabling the comparator. The counter reading is sampled at time t_6, providing the LS count to be subtracted (with the proper weight) from the digital number represented by the former MS bits. The ratio between the absolute values of the slopes of the two ramps determines the number and weight of LS bits. The value of Δt is nominally less then one clock time. Yet, in practice, due to delays in the comparator and the switching, it might reach as high as some clock times, the actual number of which depends also upon the clock frequency. Consequently, the period and the number of counter stages assigned to the second ramp is to be increased accordingly.

Being used in IR imagers, an offset thus created is compensated for in the non – uniformity correction (NUC) procedure, provided it has a constant value. An advantage associated with the ADC implementation in accordance with the present invention, results from the comparator being activated at a constant input level by a signal of a constant slope, independent of the converted signal amplitude. Also, the focal plane is cooled to a very stable temperature. Therefore, the delays and the resulting offset are very stable. Another advantage obtained by using the invented ADC in focal plane arrays is the connection of the column line to a virtual ground. The column lines are

long and parallel, resulting in a significant coupling capacitance between neighbors. During the period of transfer of charge from the pixel to the ADC, the column line potential is temporarily raised, only to revert to the original value by the end of that period. Therefore, finally no charge injection occurs between adjacent column lines.

The combination a common linear voltage ramp (**148** or **150 in Fig. 5B**) driving the capacitor **100** (in **Fig. 5A**) into the virtual ground of the integrator, enables applying low level DC current sources of approximately the same amplitude to all the ADCs. Thus the use of current mirrors, which are not accurate enough (especially in the nano-ampere levels), is avoided. The ramp generator **106** (in **Fig. 5A**) is basically an integrator, fed at each step of the conversion cycle by a constant current source of appropriate amplitude and polarity.

In order to further decrease the conversion time without loosing resolution, the "dual ramp single slope ADC" concept can be further extended into a multi ramp ADC, where additional conversion steps, having successively decreased weights, are employed. This may be desirable in the case of very high resolution converters.

Programmable logic applications in the present invention

The FPP of the present invention is applicable to IR imagers in general. Yet, it is especially advantageous in cooled imagers, where the heat dissipated in

the focal plane should be removed by cooling to a low and stable temperature. Therefore, architectural and functional considerations of the make – up of the integrated circuit have been made in order to decrease the power dissipation in the FPP integrated circuit. In accordance with one aspect of the invention, a programmable logic device, external to the dewar in which the integrated circuit of the sensor is disposed, performs several tasks. The first one relates to the digital functions of the ADCs which are partially performed outside of the dewar. These functions being performed in the uncooled environment, serve to decrease the amount of components and heat dissipation in the FPP, therefore potentially improving the overall performance of the imager. As explained above, the digital value of each pixel is obtained in a MS part and an LS part. The two parts, after initial processing in the FPP, are finally combined to form one digital word in the external programmable logic device. The second task relates to the remapping of the pixels. The data transmission from the FPP to the programmable logic is optimized to minimize focal plane power dissipation. Consequently, the bits of a digital word transmitted from the dewar include a mixture of data from two pixels. Such mixed data is remapped in the external logic device, to restore the image.

The external programmable logic device also adds flexibility and optimizes the conversion cycle. Whereas the order of succession of the various conversion steps is fixed, the duration of each step is controlled externally. Thus, the duration of each step is set as required by the actual performance sequence, avoiding the need to reserve lengthy intervals of time for confidence margins. The data transfer associated with this aspect of the

invention is described with reference to **Fig. 6**. The detector assembly **170**, includes a focal plane module **172** and an external proximity board **174**. The proximity board is a printed circuit board, placed close to the dewar pins, upon which the programmable logic such as FPGA (field programmable gate array) **176**, a clock generator **178** and power supply regulation circuits **180** are mounted. In the focal plane module **172**, the detector component **182** and the FPP **184** are included. The interconnections between the proximity board **174** and the focal plane module **172** are divided into four groups: regulated FPP power supplies bus, slow communications link, FPP clock and timing link and the raw data bus.

Through the conventional comparatively slow communication bus, various operation parameters of the FPP, which are not directly involved in the timing of the analog-to-digital conversion steps, are controlled, These include, inter alia, "integrate-then-read" (ITR) or "integrate-while-read" (IWR) modes of operation, working points, readout window size and location, etc. One parameter should be mentioned here, namely the resolution of the analog-to-digital conversion. The duration of a conversion cycle depends also on the resolution, increasing with the resolution. Some bits of the slow communication stream control the resolution, e.g. a 13bit or a 15bit resolution, enabling a trade-off between the resolution and the frame-rate.

A faster link carries to the FPP the clock signal and the timing information of the conversion steps, mentioned earlier. In this fast channel, a stream of short pulses is sent on a wire from the external programmable logic to the FPP, where each pulse is recognized in the FPP as the start or end of a specific step. Programming the intervals between the pulses, the optimal

conversion duration is determined. The raw data bus carries the partially processed data produced by the ADCs, from the FPP to be finally processed and remapped in the programmable logic device.

A different aspect of the imaging array which relates to the external programmable logic, is its exploitation as a user interface. Thus, in some embodiments of the invention, the programmable logic device can be used also as an interface to the external system **190** in **Fig. 6**, simplifying the users' interaction with the FPP. While the FPP of the invention operates with the optimal clock and timing for the conversion, the user can approach the buffered output on the programmable logic implementing specific communications protocol and clock. The clock of the user system is independent of the clock of the detector assembly, and does not have to be synchronized with it. The dialog between the two systems can then be established by an handshaking implemented on the programmable logic device.

As described so far, the system of the invention is most beneficial in cooled FPPs, typically implemented in thermal IR imaging. It is nevertheless contended that the same system can be used in any FPP systems, for other imaging purposes, such as visible, near infra - red and X – ray. In such systems, heat dissipation in the FPP may be less critical, but the benefits of the system are still evident.

CLAIMS

1. A focal plane array containing rows and columns of pixels for IR imaging, wherein pixel readout and analog to digital conversion is performed in an integrated circuit inclusive of said array, comprising:
   - at least one capacitor per pixel, for accumulating the charge of a detector element.
   - at least one analog to digital converter (ADC) incorporating a comparator for on/off switching a digital controller, wherein said controller controls a digital to analog charge converter for providing an appropriate amount of charge to cancel out the charge of one pixel at a time by one ADC, and
   - switching elements for connecting said pixels to said ADCs.

2. A focal plane array for IR imaging as in claim 1 comprising a cycle generator, for controlling a charge output of a digital to analog converter to cancel out said charge of said pixel.

3. A focal plane array for IR imaging as in claim 2 wherein said cycle generator is a ramp generator connected through a capacitor to the input port of said at least one ADC and to a column line.

4. A focal plane array for IR imaging as in claim 3 wherein said ramp generator produces at least one linear ramp.

5. A focal plane array for IR imaging as in claim 1 wherein said comparator includes an integrator as an input stage.

6. A focal plane array for IR imaging as in claim 1 and wherein said focal plane array is cooled.

7. A focal plane array for IR imaging as in claim 1 wherein said ADCs are allocated in groups, wherein all ADCs of one group operate simultaneously.

8. A focal plane array for IR imaging as in claim 7 each of said groups contain at least two ADCs per each column.

9. A focal plane array for IR imaging as in claim 7 and wherein one multi ramp generator serves at least one group of ADCs.

10. A focal plane array for IR imaging as in claim 7 and wherein one counter serves at least one group of ADC's.

11. An IR imaging system as in claim 1and wherein an external programmable logic device connected via a communication channel participates at least in the control of said ADC.

12. An IR imaging system as in claim 11 wherein said external programmable device also contains a buffer, for providing a interface between the pixels' readout stream and the timing parameters and communications protocols of a user.

13. A method for digitally quantifying IR radiation impinging on a focal plane array, wherein pixels readout and analog to digital conversion is performed in an integrated circuit inclusive of said array, employing at least one circuit for each column of said array, and wherein a charge on each of said pixels is converted to a digital number, comprising the steps of:

- on/off switching by a comparator of a digital controller controlling a digital to analog charge converter for supplying a charge by a digital to analog converter in an appropriate quantity to cancel out said charge of said pixel, and
- generating a dual ramp conversion cycle for a substantially two step analog to digital conversion of said charge and providing a most significant count in a first step and a least significant count of said charge in a second step.

14. A method for digitally quantifying IR radiation impinging on a focal plane array as in claim 13 wherein an analog to digital conversion of the charge in every pixel is done on the focal plane in two quantification steps, a first step providing the most significant bits and a second step the least significant bits of said quantification.

15. A method for digitally quantifying IR radiation impinging on a focal plane array as in claim 14 and wherein the combination of the most significant bits and the least significant bits into one digital number is done partially externally, outside said focal plane array.

16. A method for digitally quantifying IR radiation impinging on a focal plane array as in claim 13 and wherein a cycle is generated for controlling the charge output of a digital to analog converter to cancel out said charge of said pixel.

17. A method for digitally quantifying IR radiation impinging on a focal plane array as in claim 16 and wherein a cycle generated contains at least one ramp .

18. A method for digitally quantifying IR radiation impinging on a focal plane array as in claim 13, and wherein a tradeoff between the resolution of said quantification and the frame rate is enabled by programming said dual ramp conversion cycle.

19. A method for digitally quantifying IR radiation impinging on a focal plane array as in claim 13 and wherein said charge of said pixel is loaded first into a capacitor of an integrator wherein said integrator is connected to a column of said array, and wherein said charge is later digitally quantified.

20. A method for digitally quantifying IR radiation impinging on a focal plane array as in claim 13, and wherein the pixels of said array are grouped, such that quantification is performed simultaneously for all members of said group, each group at a time, allocating at one conversion time one ADC to each member of each group.

21. A method for digitally quantifying IR radiation impinging on a focal plane array as in claim 20, and wherein for said each group of pixels, one common ramp generator produces at least one linear voltage ramp whereby in each ADC a low level DC current is created by said ramp driving a capacitor connected to a virtual ground of an integrator.

22. A method for digitally quantifying IR radiation impinging on a focal plane array as in claim 20, and wherein each of said groups contain two rows of said array.

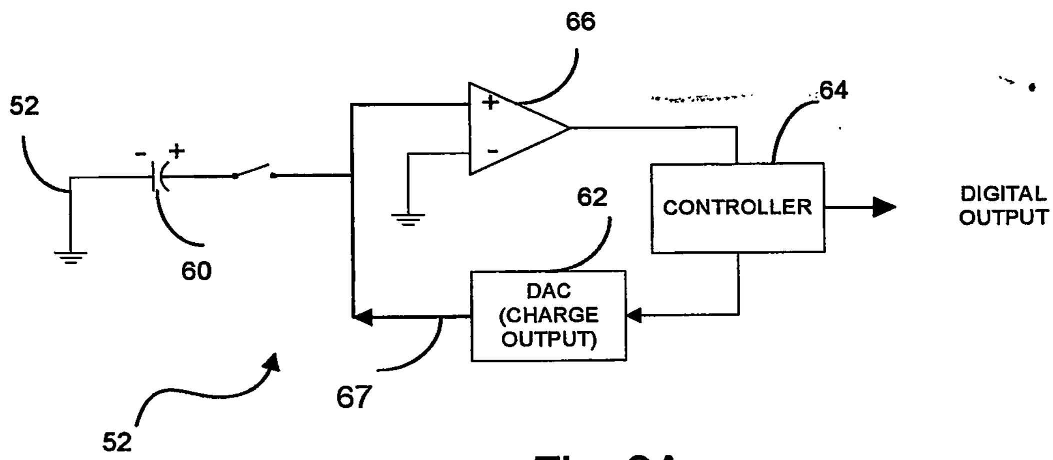


Fig. 3A

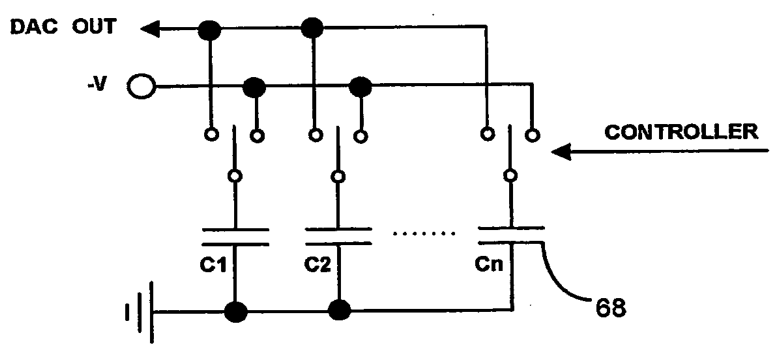


Fig. 3B

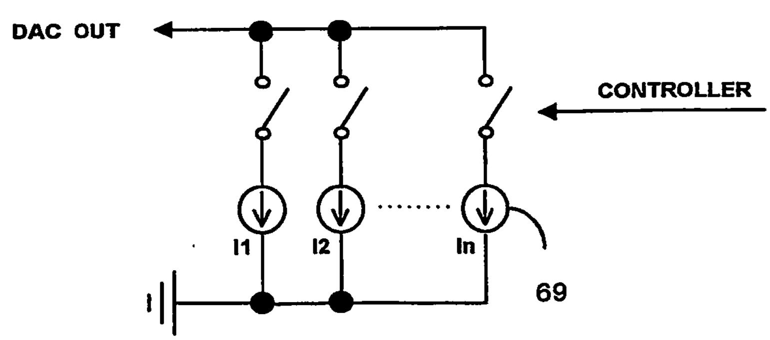


Fig. 3C

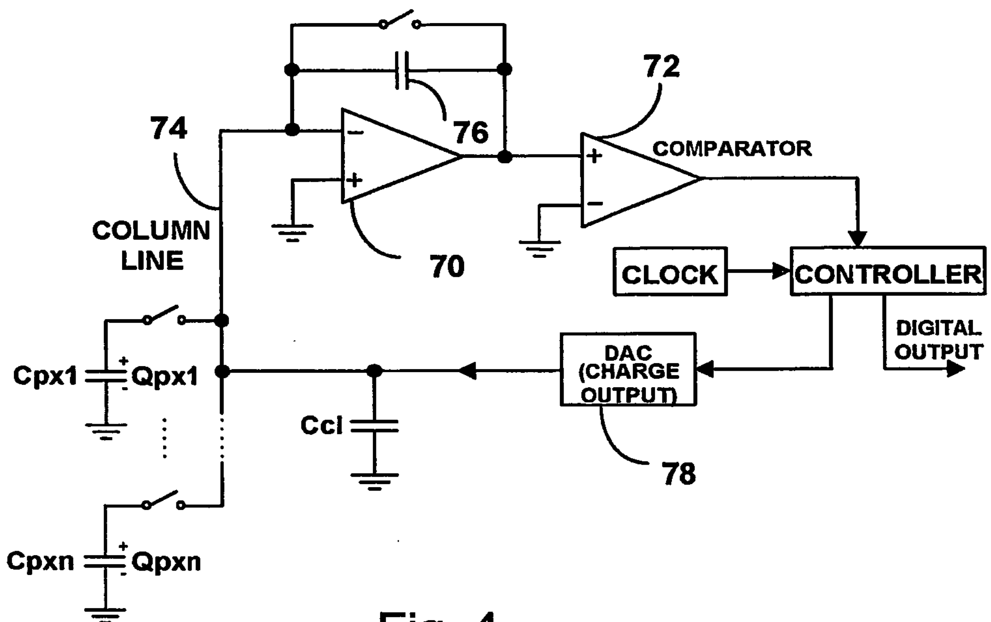
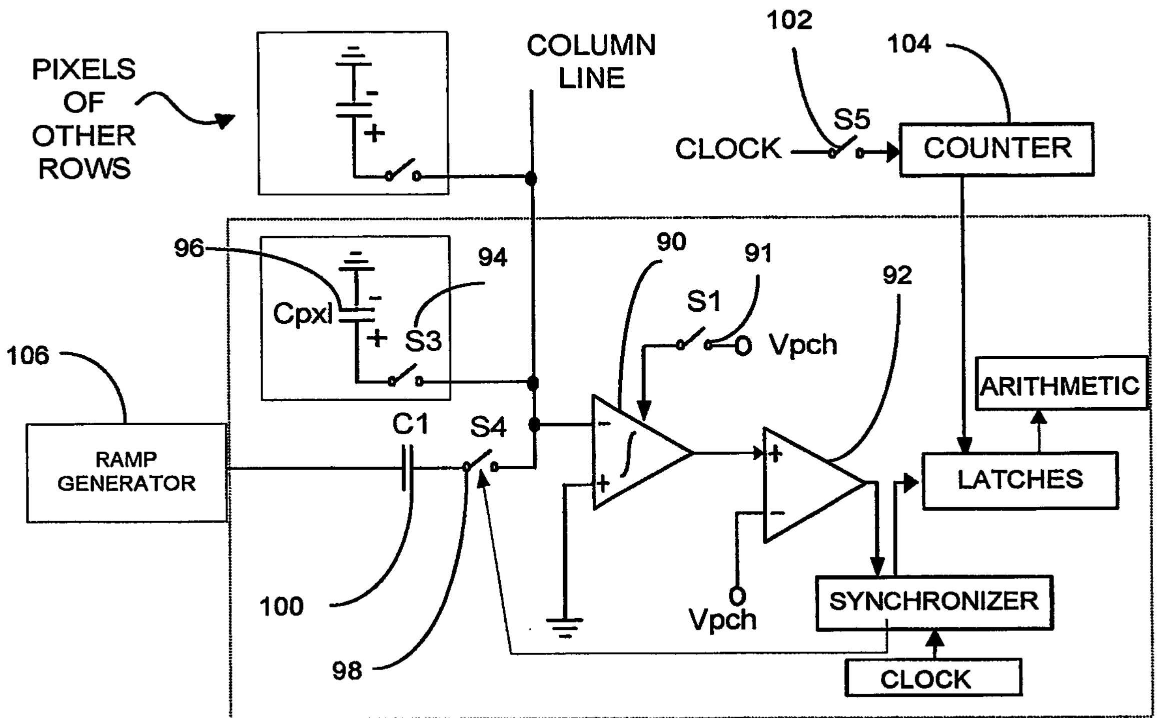

74
COLUMN LINE
76
72
COMPARATOR
70
CLOCK
CONTROLLER
DIGITAL OUTPUT
DAC (CHARGE OUTPUT)
Cpx1
Qpx1
Ccl
78
Cpxn
Qpxn

Fig. 4



PIXELS OF OTHER ROWS
COLUMN LINE
102
104
S5
CLOCK
COUNTER
96
94
90
91
92
S1
Vpch
Cpxl
S3
106
ARITHMETIC
C1
S4
RAMP GENERATOR
LATCHES
100
Vpch
SYNCHRONIZER
98
CLOCK

Fig. 5A

10/511000

6/7

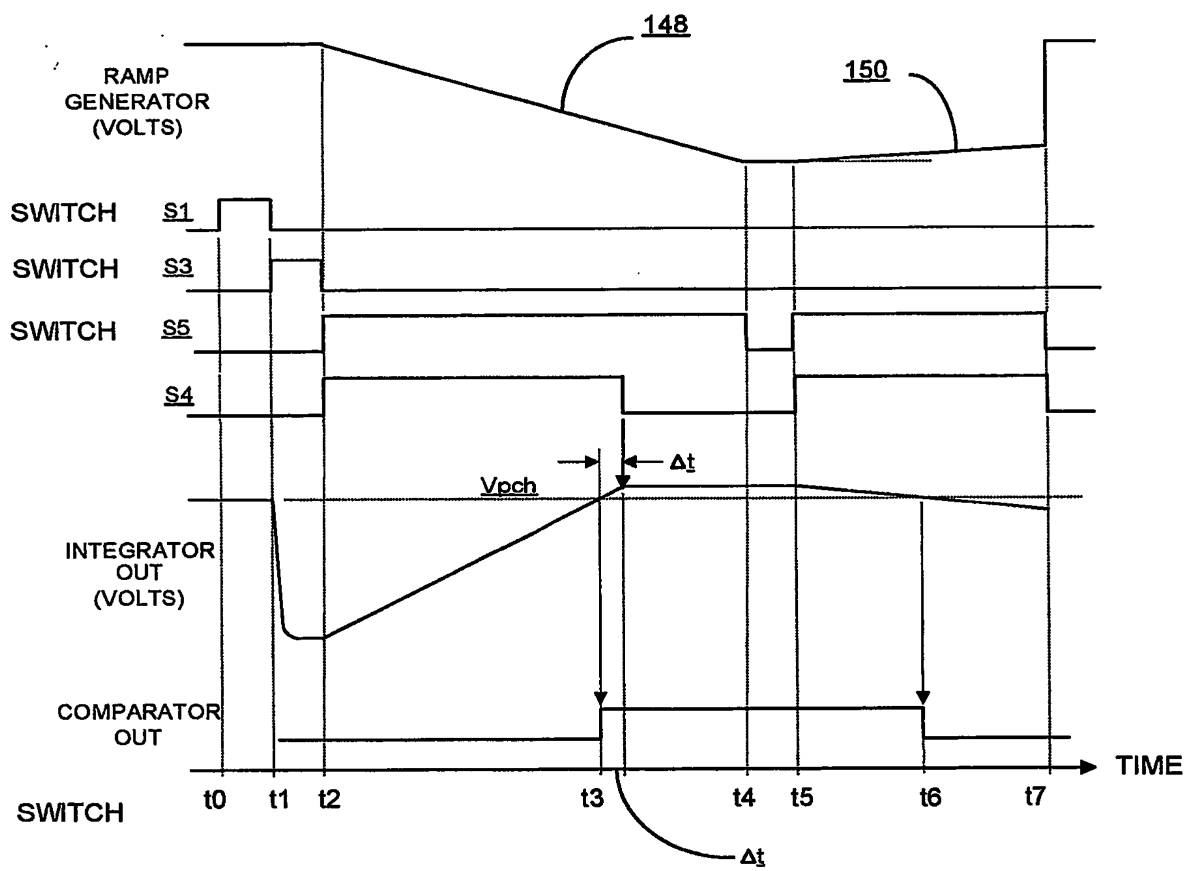


Fig. 5B

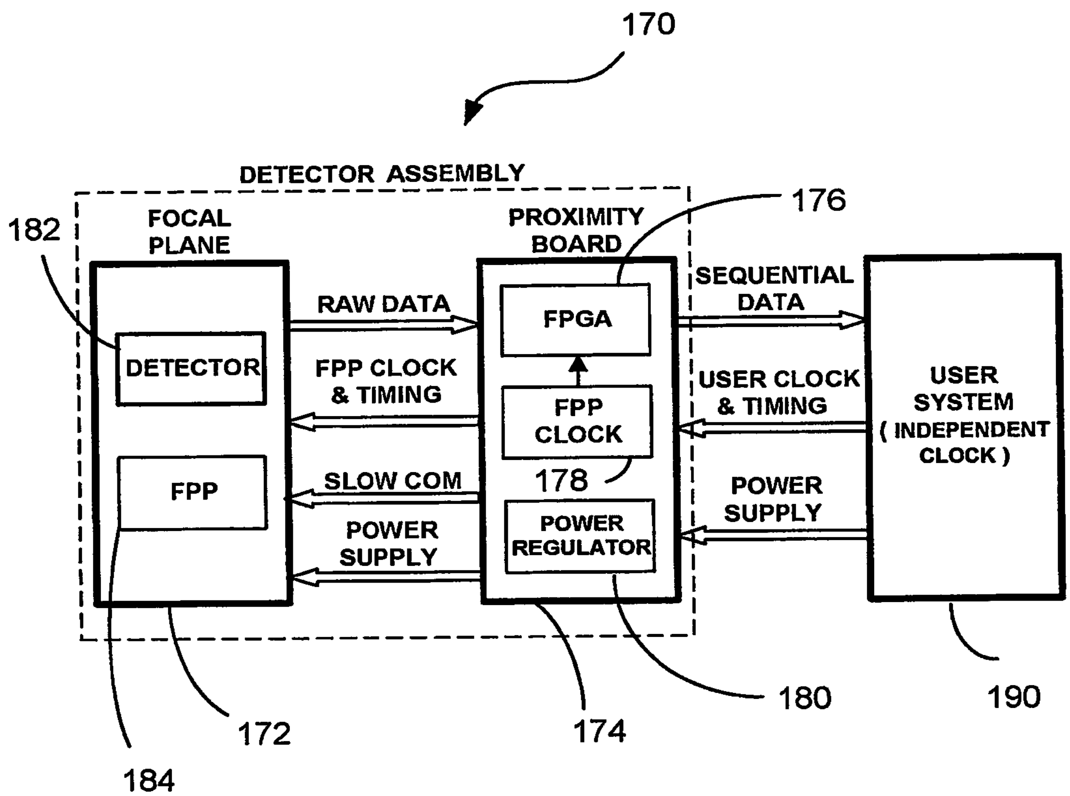

170
DETECTOR ASSEMBLY
182
FOCAL
PLANE
DETECTOR
FPP
RAW DATA
FPP CLOCK
& TIMING
SLOW COM
POWER
SUPPLY
PROXIMITY
BOARD
176
FPGA
FPP
CLOCK
178
POWER
REGULATOR
SEQUENTIAL
DATA
USER CLOCK
& TIMING
POWER
SUPPLY
USER
SYSTEM
(INDEPENDENT
CLOCK)
172
174
180
190
184

Fig. 6